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EXAMINER	
PERALTA, GINETTE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,779	HYUNG-BOK CHOI	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 3, 16 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Parekh et al. (U. S. Pat. 6,468,859 B1).

Regarding claim 1, Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer 28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines

7-11); forming a storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28.

Regarding claim 2, Parekh et al. discloses in col. 3, lines 64-65, and col. 4, lines 6-11 that the storage node contact 40 is a polysilicon plug and an upper portion of the polysilicon plug is recessed or removed at the step of forming the supporting hole 56.

Regarding claim 3, Parekh et al. discloses in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process.

Regarding claim 16, Parekh et al. discloses in Fig. 10 a capacitor for use in a semiconductor device that comprises a substrate 11; an inter-layer insulating layer 28 having a contact hole exposing a partial portion of the substrate and being formed on the substrate 11; a storage node contact 40 providing a supporting hole at an upper region of the contact hole and filling a partial portion of the contact hole; and a storage node 58 being connected to the storage node contact 40 wherein a bottom portion of the storage node is filled and secured into the supporting hole.

Regarding claim 20, Parekh et al. discloses in col. 3, lines 64-65 that the storage node contact 40 is a polysilicon plug.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Reinberg et al. (U. S. Pat. 6,403,442).

Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer 28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines 7-11); forming a

storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28; further discloses in col. 3, lines 64-65, and col. 4, lines 6-11 that the storage node contact 40 is a polysilicon plug and an upper portion of the polysilicon plug is recessed or removed at the step of forming the supporting hole 56; and in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process or to a chemical mechanical polishing.

Parekh et al. discloses the claimed invention with the exception of disclosing that the dry etching process is carried out by adopting an etch selectivity having a specific ratio of the polysilicon layer with respect to the storage node oxide layer.

Reinberg et al. discloses a method of forming a capacitor in which polysilicon is etched with a high selectivity to BPSG (borophosphosilicate glass) that is greater than about 20:1, wherein the etch selectivity of polysilicon to BPSG is taught for the disclosed intended purpose of etching the polysilicon that forms the storage node without essentially removing the BPSG that forms a storage node supporting hole.

Parekh et al. discloses that the interlayer-insulating layer comprises BPSG, while the storage node contact comprises polysilicon. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the polysilicon of the storage node contact with a high selectivity with respect to the BPSG that forms the storage node oxide layer that form part of the supporting hole in the invention of

Parekh et al., and to vary the selectivity ratio beyond the rate taught by Reinberg et al. of 20 to 1, as there is no statement denoting the criticality of the selectivity ratio if the storage node oxide layer is preserved as Parekh et al. as modified by Reinberg et al. discloses.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al. in view of Grant et al. (U. S. Pat. 6,884,722 B2).

Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer 28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a

downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines 7-11); forming a storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28; further discloses in col. 3, lines 64-65, and col. 4, lines 6-11 that the storage node contact 40 is a polysilicon plug and an upper portion of the polysilicon plug is recessed or removed at the step of forming the supporting hole 56; and in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process or to a chemical mechanical polishing.

Parekh et al. discloses the claimed invention with the exception of disclosing that the supporting hole may be formed by a wet etching process, and the chemical solutions to be used.

Grant et al. discloses in col. 4, lines 11-36, the use of wet etching processes for the patterning and/or removal of polysilicon, the method including wet etching processes including one of a chemical solution mixed with NH_4OH at a mixing ration of 1.3 and H_2O at a mixing ratio of 80, and a chemical solution mixed with HF at a mixing ratio of 1 and HNO_3 at a mixing ration of 100-200; wherein the chemical solution is put into a dipping bath in which temperature is maintained in a range of 45°C or less for about 110 minutes, and 15 to 30°C for 8 to 250 seconds, respectively.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Parekh et al. by etching the polysilicon of the storage node contact by a wet etching process and to vary the mixing ratios and temperatures within the ranges taught by Grant et al., as there is no statement denoting the criticality of the chemical solution mixing ratios, temperatures or time since the purpose of both Parekh et al. and Grant is to effectively and selectively pattern a polysilicon layer as Parekh et al. as modified by Reinberg et al. discloses.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al..

Parekh et al. discloses that the polysilicon plug 36 has an initial thickness of less than 2000 Å. But does not discloses the thickness of the polysilicon plug after the supporting hole is formed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the thickness of the polysilicon plug as long as the polysilicon plug adequately provides a contact region by which the storage node of the capacitor connects to the underlying substrate in the invention of Parekh et al. and

since Parekh et al. discloses that the thickness will be 2000 Å or less, as there is no statement denoting the criticality of the polysilicon plug.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

7. Claims 8-11, 17-19, and 21-24 are rejected under 35 U.S.C. 103(a) as being obvious over Parekh et al. in view of Oh et al. (U. S. Pat. 6,700,153 B2).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome

by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 8, Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer 28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines 7-11); forming a storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28.

Parekh et al. discloses the claimed invention with the exception of the steps of forming the storage node oxide layer constructed with a double layer of an upper layer

and a lower layer, wherein an etch selectivity ratio of the upper layer is higher than that of the lower layer; and widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating layer and a storage node contact 115, and the steps include forming a storage node oxide layer 138 constructed with a double layer of an upper layer 135 and a lower layer 130, wherein an etch selectivity ratio of the upper layer 135 formed on the inter-layer insulating layer is higher than that of the lower layer 130; forming a storage node hole 140 exposing the storage node contact 115 by etching the storage node oxide layer 138; widening a width of the storage node hole 140′ and simultaneously forming an under-cut region at the lower layer 130 of the storage node oxide layer 138 (as shown in Fig. 8); and forming a storage node 150 having a cylinder structure and being connected electrically to the storage node contact 115 as a bottom region of the storage node is supported by the under-cut region, wherein the storage node oxide layer 138 has an upper and a lower layers with different etch selectivity ratios and storage node hole is widened and an under-cut region is formed in the lower layer for the disclosed intended purpose of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition,

no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the storage node oxide layer having an upper and a lower layer, wherein an etch selectivity of the upper layer is higher than the lower layer, and widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer in the invention of Parekh et al. for the disclosed intended purpose of Oh et al. of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Regarding claim 9, Parekh et al. as modified by Oh et al. discloses that the step of widening the storage node hole and simultaneously forming the under-cut region at the lower layer of the storage node oxide layer uses a dip process using a wet chemical, as disclosed by Oh et al. in col. 6, lines 24-53.

Regarding claim 10, Parekh et al., as modified by Oh et al. discloses in col. 3, lines 64-65, and col. 4, lines 6-11 that the storage node contact 40 is a polysilicon plug and an upper portion of the polysilicon plug is recessed or removed at the step of forming the supporting hole 56.

Regarding claim 11, Parekh et al., as modified by Oh et al., discloses in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process.

Regarding claim 17, Parekh et al. discloses in Fig. 10 a capacitor for use in a semiconductor device that comprises a substrate 11; an inter-layer insulating layer 28 having a contact hole exposing a partial portion of the substrate and being formed on the substrate 11; a storage node contact 40 providing a supporting hole at an upper region of the contact hole and filling a partial portion of the contact hole; and a storage node 58 being connected to the storage node contact 40 wherein a bottom portion of the storage node is filled and secured into the supporting hole.

Parekh et al. discloses the claimed invention with the exception of a supporting layer formed on the inter-layer insulating layer and providing a step-like opening in addition to the supporting hole.

Oh et al. discloses in Fig. 9, a supporting layer formed on the inter-layer insulating layer and providing a step-like opening in addition the storage node contact 115, wherein the supporting layer is taught for the disclosed intended purpose of preventing permeation of the etchant during the etching steps to the inter-layer insulation layer as disclosed in col. 7, lines 12-25 of Oh et al..

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the structure of Parekh et al. a supporting layer like the one taught by Oh et al. for the disclosed intended purpose of protecting the

inter-layer insulation layer by preventing permeation of the etchant during the etching steps to the inter-layer insulation layer.

Regarding claim 18, Parekh et al. as modified by Oh et al. discloses that the supporting layer is a nitride layer (as disclosed by Oh et al. in col. 4, lines 41-50).

Regarding claim 19, Parekh et al., as modified by Oh et al. discloses that the polysilicon plug 36 has an initial thickness of less than 2000 Å. But does not discloses the thickness of the polysilicon plug after the supporting hole is formed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the thickness of the polysilicon plug as long as the polysilicon plug adequately provides a contact region by which the storage node of the capacitor connects to the underlying substrate in the invention of Parekh et al. and since Parekh et al. discloses that the thickness will be 2000 Å or less, as there is no statement denoting the criticality of the polysilicon plug.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Regarding claim 21, Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a storage node contact 40 connected to the substrate by passing through the inter-layer

insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming an insulation layer 54 on the inter-layer insulating layer 28, exposing the storage node contact 40(as disclosed in col. 4, lines 12-18); forming a cylindrical storage node 58 electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28.

Parekh et al. discloses the claimed invention with the exception of the steps of forming a multi-layered insulation supporting element on the inter-layer insulating layer including at least one layer providing an under-cut region and a bottom region of the storage node being inserted into the under cut region of the multi-layered insulation supporting element.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating layer and a storage node contact 115, and the steps include forming a multi-layered insulation supporting element 138 on the inter-layer insulating layer, the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element, wherein the multi-layered insulation supporting element 138 on the inter-layer insulating layer, the multi-layer insulation supporting element 138

exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element are included for the disclosed intended purpose of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form multi-layered insulation supporting element 138 on the inter-layer insulating layer, the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element in the invention of Parekh et al. for the disclosed intended purpose of Oh et al. of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Regarding claim 22, Parekh et al. as modified by Oh et al. discloses that the step of forming the multi-layered insulation supporting element includes the steps of forming a first etch barrier layer 120 on the interlayer insulating layer; forming an insulation layer 130 on the first etch barrier layer 120; forming a second etch barrier layer on the insulation layer 135; forming an under-cut region in between the first and the second barrier layers by selectively removing the insulation layer 130.

Regarding claim 23, Parekh et al. as modified by Oh et al. discloses that the step of selectively removing the insulating layer employs a wet type dip-out process, as disclosed by Oh et al. in col. 6, lines 24-53.

Regarding claim 24, Parekh et al. as modified by Oh et al. discloses that the insulation layer is an oxide layer formed through a chemical vapor deposition process (as disclosed in col. 4, lines 65-67, and the etch barrier comprise a nitride layer, as disclosed in col. 4, lines 41-50.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being obvious over Parekh et al. in view of Oh et al. as applied to claims 8-11 above, and further in view of Reinberg et al..

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject

matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer 28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines 7-11); forming a

storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28, and as disclosed in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process.

Parekh et al. discloses the claimed invention with the exception of the steps of forming the storage node oxide layer constructed with a double layer of an upper layer and a lower layer, wherein an etch selectivity ratio of the upper layer is higher than that of the lower layer; and widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating layer and a storage node contact 115, and the steps include forming a storage node oxide layer 138 constructed with a double layer of an upper layer 135 and a lower layer 130, wherein an etch selectivity ratio of the upper layer 135 formed on the inter-layer insulating layer is higher than that of the lower layer 130; forming a storage node hole 140 exposing the storage node contact 115 by etching the storage node oxide layer 138; widening a width of the storage node hole 140' and simultaneously forming an under-cut region at the lower layer 130 of the storage node oxide layer 138 (as shown in Fig. 8); and forming a storage node 150 having a cylinder structure and being connected electrically to the storage node contact 115 as a bottom region of the storage node is

supported by the under-cut region, wherein the storage node oxide layer 138 has an upper and a lower layers with different etch selectivity ratios and storage node hole is widened and an under-cut region is formed in the lower layer for the disclosed intended purpose of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the storage node oxide layer having an upper and a lower layer, wherein an etch selectivity of the upper layer is higher than the lower layer, and widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer in the invention of Parekh et al. for the disclosed intended purpose of Oh et al. of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Parekh et al., as modified by Oh et al. above, discloses the claimed invention with the exception of disclosing that the dry etching process is carried out by adopting

an etch selectivity having a specific ratio of the polysilicon layer with respect to the storage node oxide layer.

Reinberg et al. discloses a method of forming a capacitor in which polysilicon is etched with a high selectivity to BPSG (borophosphosilicate glass) that is greater than about 20:1, wherein the etch selectivity of polysilicon to BPSG is taught for the disclosed intended purpose of etching the polysilicon that forms the storage node without essentially removing the BPSG that forms a storage node supporting hole.

Parekh et al. discloses that the interlayer-insulating layer comprises BPSG, while the storage node contact comprises polysilicon. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the polysilicon of the storage node contact with a high selectivity with respect to the BPSG that forms the storage node oxide layer that form part of the supporting hole in the invention of Parekh et al., and to vary the selectivity ratio beyond the rate taught by Reinberg et al. of 20 to 1, as there is no statement denoting the criticality of the selectivity ratio if the storage node oxide layer is preserved as Parekh et al. as modified by Reinberg et al. discloses.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

9. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being obvious over Parekh et al. in view of Oh et al. as applied to claims 8-11 above, and further in view of Grant et al..

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Parekh et al. discloses in Figs. 1 to 7 a method for fabricating a capacitor of a semiconductor device that comprises the steps of forming an inter-layer insulating layer 28 on a substrate 11 (as disclosed in col. 3, lines 20-27); forming a contact hole 38 exposing a partial portion of the substrate 11 by etching the inter-layer insulating layer

28 (as disclosed in col. 3, lines 28-37); forming a storage node contact 40 buried into the contact hole 38 such that the surface of the storage node contact 40 is at the same plane level as the surface of the inter-layer insulating layer 28 (as shown in Fig. 4 and as disclosed in col. 3, lines 49-53); forming a storage node oxide layer 54 on the inter-layer insulating layer 28 (as disclosed in col. 4, lines 12-18); forming a storage node hole 56 exposing the storage node contact 40 by etching the storage node oxide layer 54 (as disclosed in col. 4, lines 16-18); forming a supporting hole 56 having a hollow form in a downward direction by partially removing an upper portion of the storage node contact 40 exposed by the storage node hole 56 (as disclosed in col. 4, lines 7-11); forming a storage node 58 having a cylinder structure electrically connected to the storage node contact 40 wherein a bottom portion of the storage node 58 is disposed in the supporting hole 56 supported by the supporting hole 56 and the inter-layer insulating layer 28, and as disclosed in col. 4, lines 3-5 that the step of forming the supporting hole 56, the upper portion of the polysilicon plug 40 is subjected to a dry etching process.

Parekh et al. discloses the claimed invention with the exception of the steps of forming the storage node oxide layer constructed with a double layer of an upper layer and a lower layer, wherein an etch selectivity ratio of the upper layer is higher than that of the lower layer; and widening a width of the storage node hole and simultaneously forming an under-cut region at the lower layer of the storage node oxide layer.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating

layer and a storage node contact 115, and the steps include forming a storage node oxide layer 138 constructed with a double layer of an upper layer 135 and a lower layer 130, wherein an etch selectivity ratio of the upper layer 135 formed on the inter-layer insulating layer is higher than that of the lower layer 130; forming a storage node hole 140 exposing the storage node contact 115 by etching the storage node oxide layer 138; widening a width of the storage node hole 140' and simultaneously forming an under-cut region at the lower layer 130 of the storage node oxide layer 138 (as shown in Fig. 8); and forming a storage node 150 having a cylinder structure and being connected electrically to the storage node contact 115 as a bottom region of the storage node is supported by the under-cut region, wherein the storage node oxide layer 138 has an upper and a lower layers with different etch selectivity ratios and storage node hole is widened and an under-cut region is formed in the lower layer for the disclosed intended purpose of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the storage node oxide layer having an upper and a lower layer, wherein an etch selectivity of the upper layer is higher than the lower layer, and widening a width of the storage node hole and simultaneously forming an under-

cut region at the lower layer of the storage node oxide layer in the invention of Parekh et al. for the disclosed intended purpose of Oh et al. of increasing the height of the storage electrode while avoiding twin-bit failures, and ensuring a large critical dimension at the bottom of the storage electrode that is sufficiently large to satisfy capacitance requirements and in addition, no special dielectric material is needed to increase capacitance, as disclosed by Oh et al. in col. 12, lines 37-50.

Parekh et al., as modified by Oh et al., discloses the claimed invention with the exception of disclosing that the supporting hole may be formed by a wet etching process, and the chemical solutions to be used.

Grant et al. discloses in col. 4, lines 11-36, the use of wet etching processes for the patterning and/or removal of polysilicon, the method including wet etching processes including one of a chemical solution mixed with NH_4OH at a mixing ration of 1.3 and H_2O at a mixing ratio of 80, and a chemical solution mixed with HF at a mixing ratio of 1 and HNO_3 at a mixing ration of 100-200; wherein the chemical solution is put into a dipping bath in which temperature is maintained in a range of 45°C or less for about 110 minutes, and 15 to 30°C for 8 to 250 seconds, respectively.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Parekh et al. by etching the polysilicon of the storage node contact by a wet etching process and to vary the mixing ratios and temperatures within the ranges taught by Grant et al., as there is no statement denoting the criticality of the chemical solution mixing ratios, temperatures

or time since the purpose of both Parekh et al. and Grant is to effectively and selectively pattern a polysilicon layer as Parekh et al. as modified by Reinberg et al. discloses.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

10. Claims 25-27, and 30 are rejected under 35 U.S.C. 103(a) as being obvious over Kwok et al. (U. S. Pat. 6,627,938 B2) in view of Oh et al. (U. S. Pat. 6,700,153 B2).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome

by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 25, Kwok et al. discloses in Figs. 3-10 a method for fabricating a capacitor of a semiconductor device that comprises forming an inter-layer insulating layer 56 on a substrate; forming a storage node contact 58 connected to the substrate 52 by passing through the inter-layer insulating layer 56; forming a storage node supporting layer on the inter-layer insulating layer 56 such that an insulation layer 64 is inserted into a space between an etch barrier 66 and the inter-layer insulating layer 56; forming a storage node insulating layer 68 on the storage node supporting layer; forming a storage node hole 70 by etching the storage node insulating layer 68 and the storage node supporting layer to make an etching process stop at the inter-layer insulating layer 56; removing selectively the storage node insulating layer 68 and the storage node supporting layer to widen a width of the storage node hole and simultaneously form an under-cut region 72 in between the second etch barrier layer 66 and the inter-layer insulating layer 56; forming a cylindrical storage node 80 connected to the storage node contact 58 as a bottom region of the storage node formed in the storage node hole is inserted into the under-cut region 72; and removing selectively the storage node insulating layer 68.

Kwok et al. discloses the claimed invention with the exception of the storage node supporting layer having a first etch barrier layer underlying the insulation layer and on the inter-layer insulation layer.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating layer and a storage node contact 115, and the steps include forming the multi-layered insulation supporting element includes the steps of forming a first etch barrier layer 120 on the interlayer insulating layer; forming an insulation layer 130 on the first etch barrier layer 120; and forming a second insulating layer 135; forming an under-cut region in between the first and the second barrier layers by selectively removing the insulation layer 130; the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element, wherein the multi-layered insulation supporting element 138 on the inter-layer insulating layer, the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element wherein the first barrier layer is located between the inter-layer insulating layer and the insulation layer of the storage node supporting layer for the disclosed intended purpose of preventing permeation of the etchant during the etching steps to the inter-layer insulation layer as disclosed in col. 7, lines 12-25 of Oh et al..

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the structure of Kwok et al. a first barrier layer like the one taught by Oh et al. for the disclosed intended purpose of protecting the inter-layer insulation layer by preventing permeation of the etchant during the etching steps to the inter-layer insulation layer.

Regarding claim 26, Kwok et al. as modified by Oh et al. discloses that the step of widening the width of the storage node hole and forming the undercut region in between the second etch barrier layer and the first etch barrier layer, the storage node insulating layer and the storage node supporting layer are selectively etched through a wet type dip-out process, as disclosed by Oh et al. in col. 6, lines 24-53.

Regarding claim 27, Kwok et al. as modified by Oh et al. discloses that the storage node insulating layer and the storage node supporting layer are oxide layers as disclosed by Kwok et al. in col. 3, lines 35-44, and Oh et al. in col. 4, line 59-67; and the first and second etch barrier layers are nitride layers, as disclosed by Kwok et al. in col. 3, lines 35-44 and Oh et al. in col. 4, lines 48-49.

Regarding claim 30, Kwok et al., as modified by Oh et al., discloses in col. 3, lines 45-51 that the step of forming the storage node hole is carried out by employing a dry etching process.

11. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being obvious over Kwok et al. in view of Oh et al. and Grant et al..

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Kwok et al. discloses in Figs. 3-10 a method for fabricating a capacitor of a semiconductor device that comprises forming an inter-layer insulating layer 56 on a substrate; forming a storage node contact 58 connected to the substrate 52 by passing through the inter-layer insulating layer 56; forming a storage node supporting layer on the inter-layer insulating layer 56 such that an insulation layer 64 is inserted into a space between an etch barrier 66 and the inter-layer insulating layer 56; forming a storage node insulating layer 68 on the storage node supporting layer; forming a storage node

hole 70 by etching the storage node insulating layer 68 and the storage node supporting layer to make an etching process stop at the inter-layer insulating layer 56; removing selectively the storage node insulating layer 68 and the storage node supporting layer to widen a width of the storage node hole and simultaneously form an under-cut region 72 in between the second etch barrier layer 66 and the inter-layer insulating layer 56; forming a cylindrical storage node 80 connected to the storage node contact 58 as a bottom region of the storage node formed in the storage node hole is inserted into the under-cut region 72; and removing selectively the storage node insulating layer 68.

Kwok et al. discloses the claimed invention with the exception of the storage node supporting layer having a first etch barrier layer underlying the insulation layer and on the inter-layer insulation layer.

Oh et al. discloses in Figs. 6-11 a method for fabricating a capacitor of a semiconductor device that comprises a substrate 100 having an interlayer insulating layer and a storage node contact 115, and the steps include forming the multi-layered insulation supporting element includes the steps of forming a first etch barrier layer 120 on the interlayer insulating layer; forming an insulation layer 130 on the first etch barrier layer 120; and forming a second insulating layer 135; forming an under-cut region in between the first and the second barrier layers by selectively removing the insulation layer 130; the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage

node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element, wherein the multi-layered insulation supporting element 138 on the inter-layer insulating layer, the multi-layer insulation supporting element 138 exposing the storage node contact 115 and including at least one layer 130 providing an under-cut region; and forming a cylindrical storage node 150 electrically connected to the storage node contact 115 as a bottom region of the storage node is inserted into the under-cut region of the multi-layered insulation supporting element wherein the first barrier layer is located between the inter-layer insulating layer and the insulation layer of the storage node supporting layer for the disclosed intended purpose of preventing permeation of the etchant during the etching steps to the inter-layer insulation layer as disclosed in col. 7, lines 12-25 of Oh et al..

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the structure of Kwok et al. a first barrier layer like the one taught by Oh et al. for the disclosed intended purpose of protecting the inter-layer insulation layer by preventing permeation of the etchant during the etching steps to the inter-layer insulation layer.

Kwok et al., as modified by Oh et al., discloses the claimed invention with the exception of disclosing that the supporting hole may be formed by a wet etching process, and the chemical solutions to be used.

Grant et al. discloses in col. 4, lines 11-36, the use of wet etching processes for the patterning and/or removal of polysilicon, the method including wet etching processes

including one of a chemical solution mixed with NH_4OH at a mixing ration of 1.3 and H_2O at a mixing ratio of 80, and a chemical solution mixed with HF at a mixing ratio of 1 and HNO_3 at a mixing ration of 100-200; wherein the chemical solution is put into a dipping bath in which temperature is maintained in a range of 45°C or less for about 110 minutes, and 15 to 30°C for 8 to 250 seconds, respectively.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Kwok et al., as modified by Oh et al., by etching the polysilicon of the storage node contact by a wet etching process and to vary the mixing ratios and temperatures within the ranges taught by Grant et al., as there is no statement denoting the criticality of the chemical solution mixing ratios, temperatures or time since the purpose of both Kwok et al. and Grant is to effectively and selectively pattern a polysilicon layer.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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